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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,131	12/03/2001	Ji Soo Park	0465-0881P	5713

2292 7590 03/09/2004

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EXAMINER	
KESHAVAN, BELUR V	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 03/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,131	PARK ET AL.	
	Examiner	Art Unit	
	Belur V Keshavan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/377,495.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status Of Claims

Claims 1, 4 and 10 have been amended. Claim 21 has been cancelled. Claims 1-20 are in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-9 and 10-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle et al. (U. S. Patent No: 6,022,524) in view of Broadbent et al. (IEEE Transactions on Electron Devices Vol. 36. No.11, November 1989).

Doyle et al. disclose a method of forming a gate in semiconductor device comprising:

Forming a first insulating film and a non-silicide conductive film of polysilicon layer (claim 5) in column in column 2, lines 48-53, on a semiconductor substrate;

Patterning the first insulating film and the conductive film to form a gate wherein the top and side surfaces of the gate are exposed in column 3, lines 59-63.

Forming a second insulating film thicker than the gate on the exposed top and side surfaces of the non-silicide gate and on the entire surface of the substrate, in column 2, lines 60-61 and in column 3, lines 10-13.

Planarizing the second insulating film to expose the top surface of the gate electrode by CMP process (claim 9) in column 3, lines 10-14;

Depositing a metal layer on an entire surface such that the metal layer is in contact with the top surface of the gate in column 3, lines 16-17, lines 58-63 and lines 30-33 in column 1;

Forming silicide on an upper surface of the gate by heat treatment in column 3, line 19;

Etching the metal layer and the second insulating film in column 3 and lines 32-33.

Regarding claims 1, 4 and 10, Doyle et al. lack use of a non-silicide gate only in the disclosed embodiments before depositing a gate metal to form gate metal silicide. However, Doyle et al. do teach, in column 3, lines 60-63, that it is not a requirement for their invention that source and drain be silicided and therefore that gate can be only non silicide gate till a gate metal is used to form gate metal silicide. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use only non-silicide gate till gate metal used to form the gate metal silicide as it would simplify the process of forming gate.

Regarding claims 1 and 2, Doyle et al. lack an explicit use of a refractory metal in the disclosed embodiments. However Doyle et al. do teach, in column 3, lines 45-61, the use of any metal that could form a low resistance silicide with polysilicon and suggest, in column 1, lines 31-33, the use of refractory metal silicide as a conductor. Additionally Broadbent teaches the

benefits of using cobalt silicide wherein cobalt is a refractory metal. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a refractory metal such as cobalt to form a low resistance and stable silicide with polysilicon as cobalt silicide reduces the time constant of the gate and that of the lines which in turn make the operation of the device and the circuit faster with high reliability and thermal stability.

Regarding claims 1 and 10, Doyle et al. disclose the claimed invention of forming a second insulating film thicker than the gate on the exposed top and side surfaces of the gate and on the entire surface of the substrate except forming a second insulating film having a potion above the gate that is thicker than the gate, and a potion on the entire surface of the substrate that is thicker than the gate. It would have been an obvious matter of design choice to form a second insulating film having a potion above the gate that is thicker than the gate, and a potion on the entire surface of the substrate that is thicker than the gate, since the applicants have not disclosed that forming a second insulating film having a potion above the gate that is thicker than the gate, and a potion on the entire surface of the substrate that is thicker than the gate solves any stated problem or is for any particular purpose. Further as applicants and Doyle et al. disclose of planarizing the second insulating film after its formation to expose the top surface of the gate it appears that the invention would perform equally well the teachings of Doyle et al.

Regarding claims 3 and 6, Doyle et al. lack thickness of cobalt as 300 angstroms and polysilicon thickness of 2500 angstrom. Broadbent teaches on page 2441 deposition of cobalt in the range from 140 to 400 angstroms and use of 0.5 microns of polysilicon to form cobalt silicide for gate and interconnection. It would have been obvious to one having an ordinary skill in the art at the time the invention was made to use 300 angstroms of cobalt and 2500 angstroms of

polysilicon, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.*

Regarding claim 4, Doyle teaches a method of forming gate sidewalls by etching and leaving an insulating film at the sides of the gate at any stage of processing in column 2, lines 48-53.

Regarding claims 7 and 8, Doyle et al. lack the heat treatment for forming silicide at temperature of 400-800°C and the use of wet etch using HCl based solution to remove the nonreacted cobalt metal layer. Broadbent et al. teach on page 2441 formation of cobalt silicide by heat treatment at 700°C that is within the claimed temperature range and teach on page 2441 wet etching the un-reacted refractory metal using HCl based solution. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Doyle and that of Broadbent to form claimed cobalt silicide to obtain low electrical resistance and to have thermal stability and reliability of the silicide and to wet etch the non-reacted refractory metal.

Regarding claims 10, 11, 13 and 14 Doyle et al. disclose a method of fabricating a gate in a semiconductor device comprising:

Forming a non-silicide conductive pattern of polysilicon (claims11 and 13) on a semiconductor substrate in column 3, lines 15-17; forming an insulating layer on and around the polysilicon pattern (claim 14) in column 3, lines 10-12; and etching the polysilicon layer to the predetermined width (claim 13) in column 3, lines 17-18.

Planarizing the insulating layer to expose the polysilicon pattern before forming the refractory metal on the polysilicon layer (claim 14) in column 3, lines 12-14.

Forming a refractory metal silicide pattern on the conductive pattern after the conductive pattern is formed by heat treating the refractory metal formed on the conductive pattern such that the refractory metal is adjacent to the conductive pattern and the silicide pattern having the predetermined width at an intersection between the refractory metal and the conductive metal in column 3, lines 17-19 and in column 1, lines 31-33.

Regarding claim 17, Doyle et al. disclose the method:

Forming a gate insulating layer on the semiconductor substrate in column 2, line 49; forming the polysilicon layer on the gate insulating layer in column 2 lines 51-52; and forming a gate insulating pattern by etching the gate insulating layer to the predetermined width in column 2, line 49 and in figure 1(a) (106).

Regarding claim 18, Doyle et al. disclose in columns 2 and 3 and in figure 1(a) (106 and 104) wherein the polysilicon layer and the gate insulating layer are respectively etched to form polysilicon pattern and the gate insulating pattern before the silicide pattern is formed.

Regarding claim 19, Doyle et al. disclose in figure 1(e) a method wherein the sides of the gate insulating layer, the polysilicon pattern and silicide pattern are aligned orthogonal to a surface of the semiconductor substrate on which the gate insulating film is formed.

Regarding claim 20, Doyle et al. disclose in column 2 lines 52-53 forming a gate sidewall on at least one side of the gate insulating layer, the polysilicon pattern and the silicide pattern.

Regarding claims 10 and 15, Doyle et al. lack an explicit use of a refractory metal in the disclosed embodiments. However Doyle et al. do teach, in column 3, lines 45-61, the use of any

metal that could form a low resistance silicide with polysilicon and suggest, in column 1, lines 31-33, the use of refractory metal silicide as a conductor. Additionally Broadbent teaches the benefits of using cobalt silicide wherein cobalt is a refractory metal. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a refractory metal such as cobalt to form a low resistance and stable silicide with polysilicon as cobalt silicide reduces the time constant of the gate and that of the lines which in turn make the operation of the device and the circuit faster with high reliability and thermal stability.

Regarding claims 12 and 16, Doyle et al. lack thickness of cobalt as 300 angstroms and polysilicon thickness of 2500 angstrom. Broadbent teaches on page 2441 deposition of cobalt in the range from 140 to 400 angstroms and use of 0.5 microns of polysilicon to form cobalt silicide for gate and interconnection. It would have been obvious to one having an ordinary skill in the art at the time the invention was made to use 300 angstroms of cobalt and 2500 angstroms of polysilicon, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.*

Response to Arguments

The examiner has noted amendments to claims 1, 4 and 10 and cancellation of claim 21

Applicants' remarks on the rejection of claims 1-20 under 35 U.S.C 103 filed on 02/02/04 have been fully considered but they are not persuasive. .

The examiner notes the applicants' argument that Doyle fails to disclose or suggests a combination of elements in a method of forming a gate in a semiconductor device.

Doyle et al. teach in column 3 and lines 55-65 that in their invention it is not requirement that source/drain regions be silicided which means that the first silicide layer (110) is not needed. Therefore the sacrificial dielectric layer (114) will make a contact with the surface of the gate. Further, Doyle et al. disclose forming a dielectric (114) on the exposed top and side surfaces and on the entire surface of the substrate and planarizing the substrate by CMP to expose the top surface of the gate electrode through the dielectric layer. Therefore it is obvious that the dielectric layer is thicker than the gate and it is also shown in figure 1(b). Doyle et al. disclose forming subsequently gate silicide on the exposed gate electrode, which reduces the gate resistance. Further, layer 110 is formed "concurrently" with layer 112. If layer 112 is not formed as suggested by Doyle, then the layer 110 is also not formed. The embodiment which includes 110 is just "an embodiment" and not the only embodiment suggested. Also Doyle et al. teach that that in their invention the sidewall spacers are not required.

Applicants' Remarks of 2/2/2004 requesting for reconsideration of the application and withdrawal of the rejection have been fully considered and are not persuasive for the reasons given above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Belur V Keshavan whose telephone number is 571-272-1894. The examiner can normally be reached on 8-4:30 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bvk.
March 2, 2004.

Belur V. Keshavan
Examiner. Art Unit 2825.

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800